Incremental checkpointing of program state to NVRAM for transiently-powered systems

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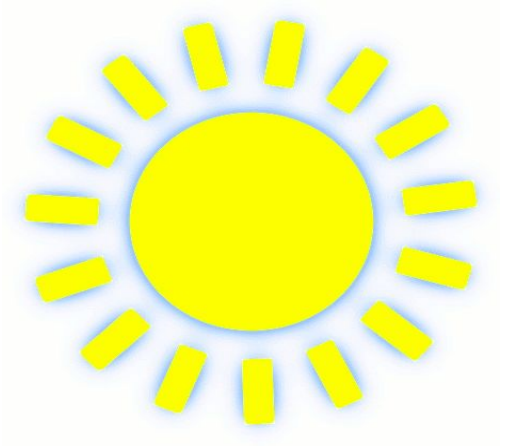
IoT constraints

Autonomous

Small

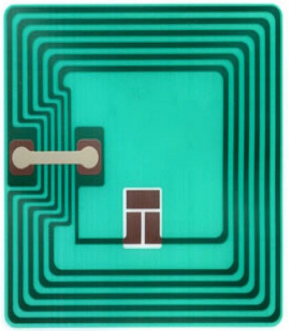
Cheap

Harvesting from solar



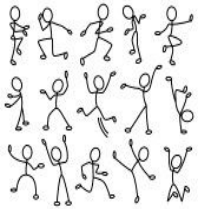
Size 

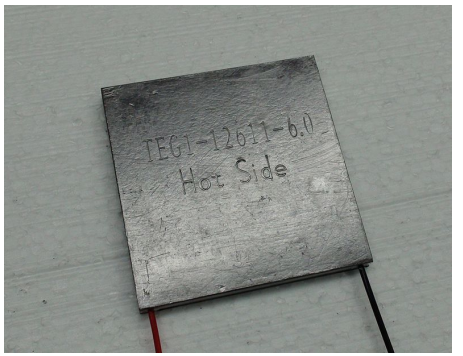
Harvesting from RF

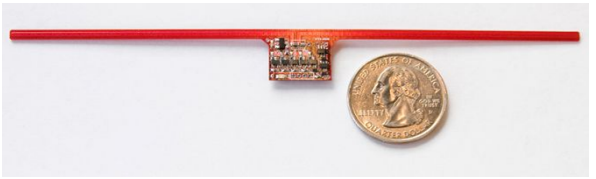


Constrain applications

Emerging platforms







Intel WISP
[Sensys 2008]

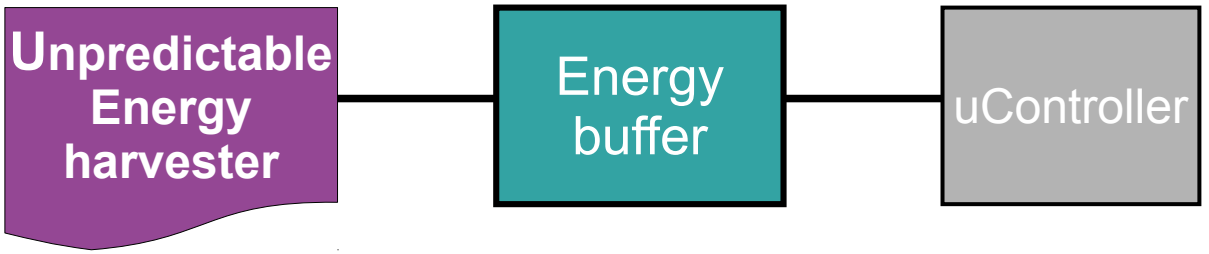
Unpredictable

Harvesting from unpredictable sources

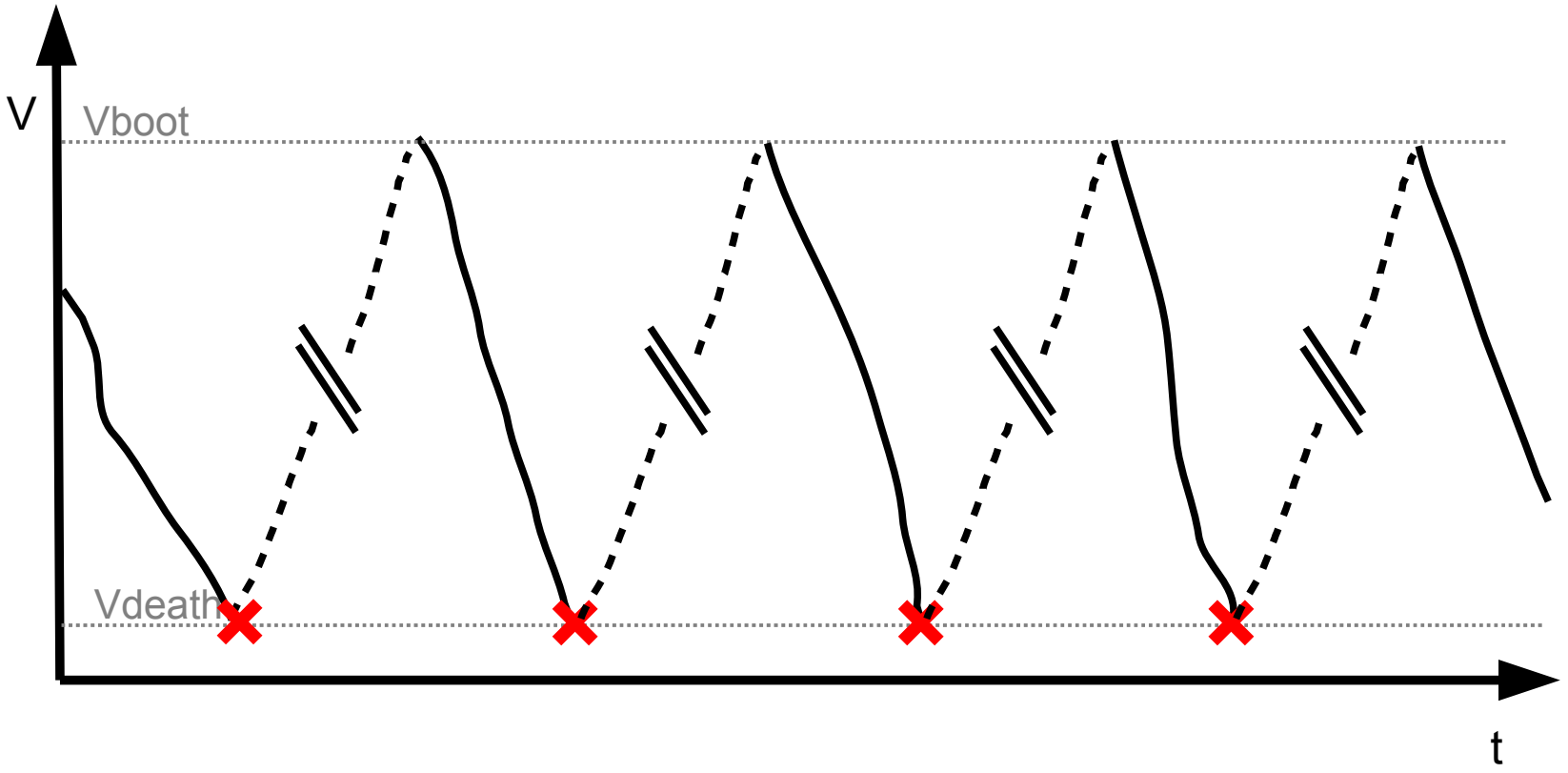
- Low power

  →Small energy buffer
- Harvested energy is unpredictable

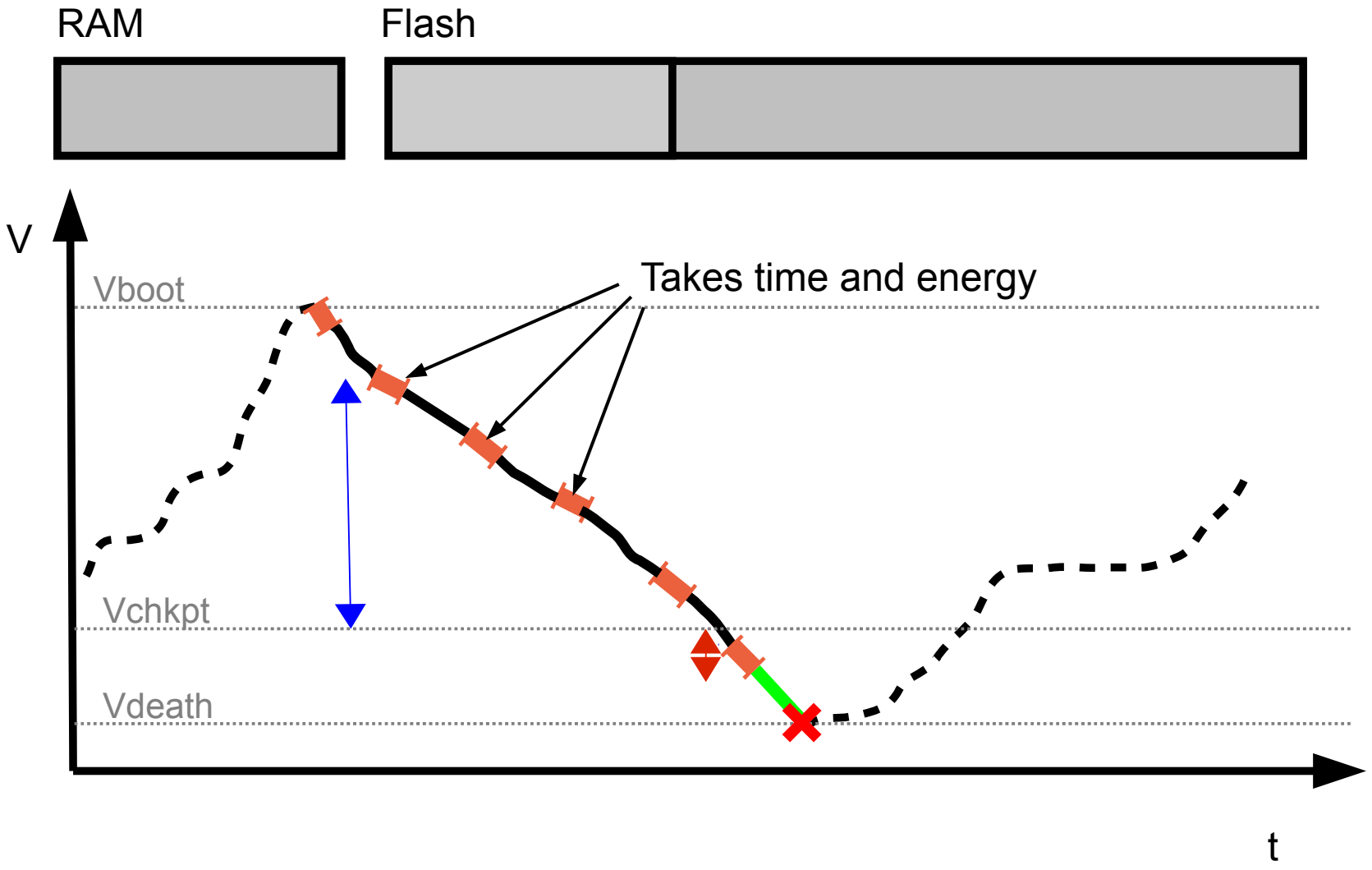
  → Frequent outages → Frequent reboots



Harvesting from chaotic sources



Mementos [ASPLOS 2011]



NVRAMs

- ✔ Retains data when not powered
- ✔ Directly addressable
- ✔ Low latencies/consumption (w.r.t. Flash)

 Why not a full-NVRAM memory architecture ?

- ✗ NVRAM not as efficient as SRAM
- ✗ Not crash-proof

We argue for a NVRAM + SRAM architecture

→ [TI FRAM Series, 2013]

Plan

I. Introduction

II. Contribution

III. Validation

Contribution

Goal: build a reboot-proof system for a SRAM + NVRAM memory architecture

Two tasks:

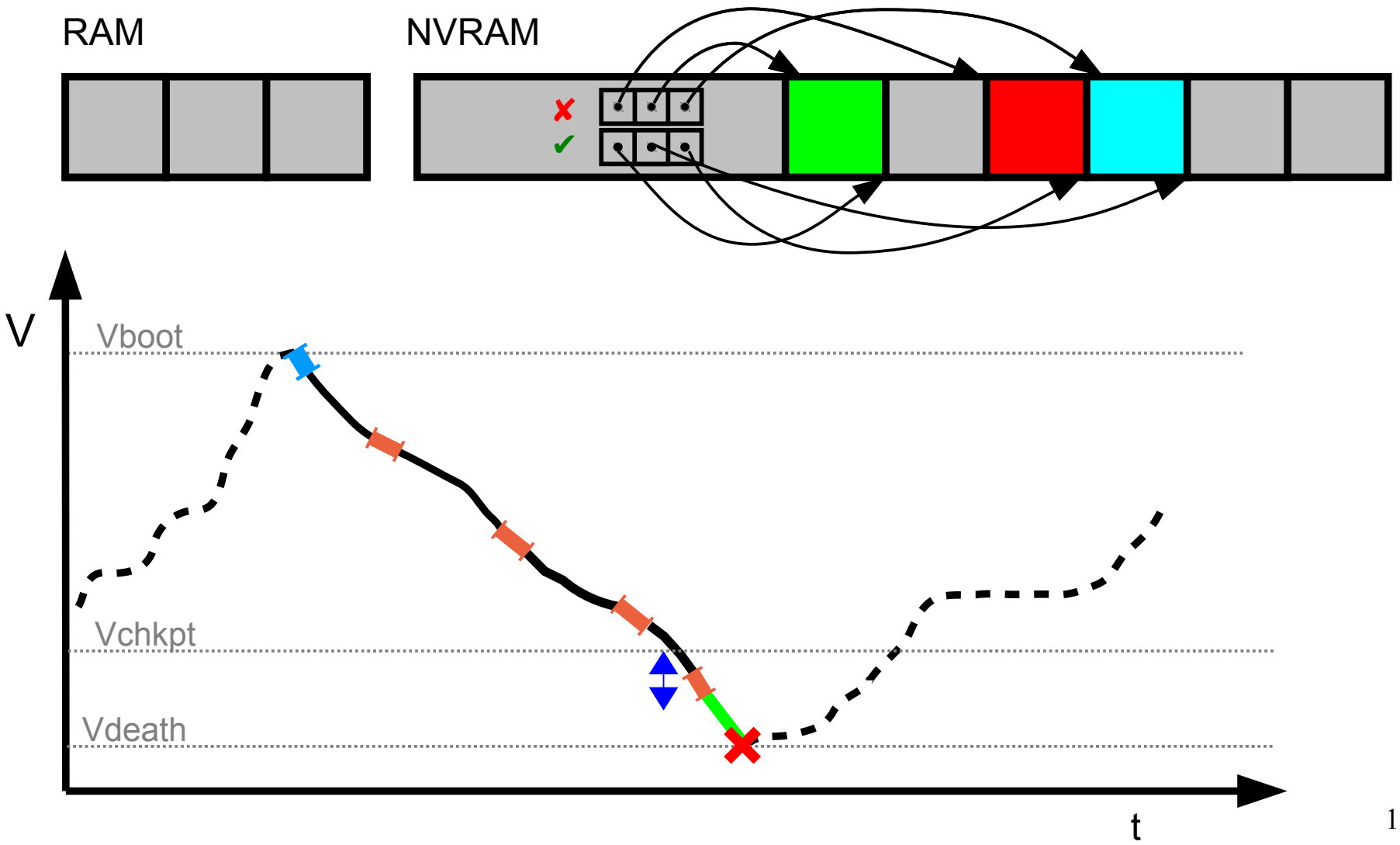
(1) Saving the system state before a power-failure

→ On a SRAM + NVRAM architecture

(2) Doing so at the right time

→ With low overhead

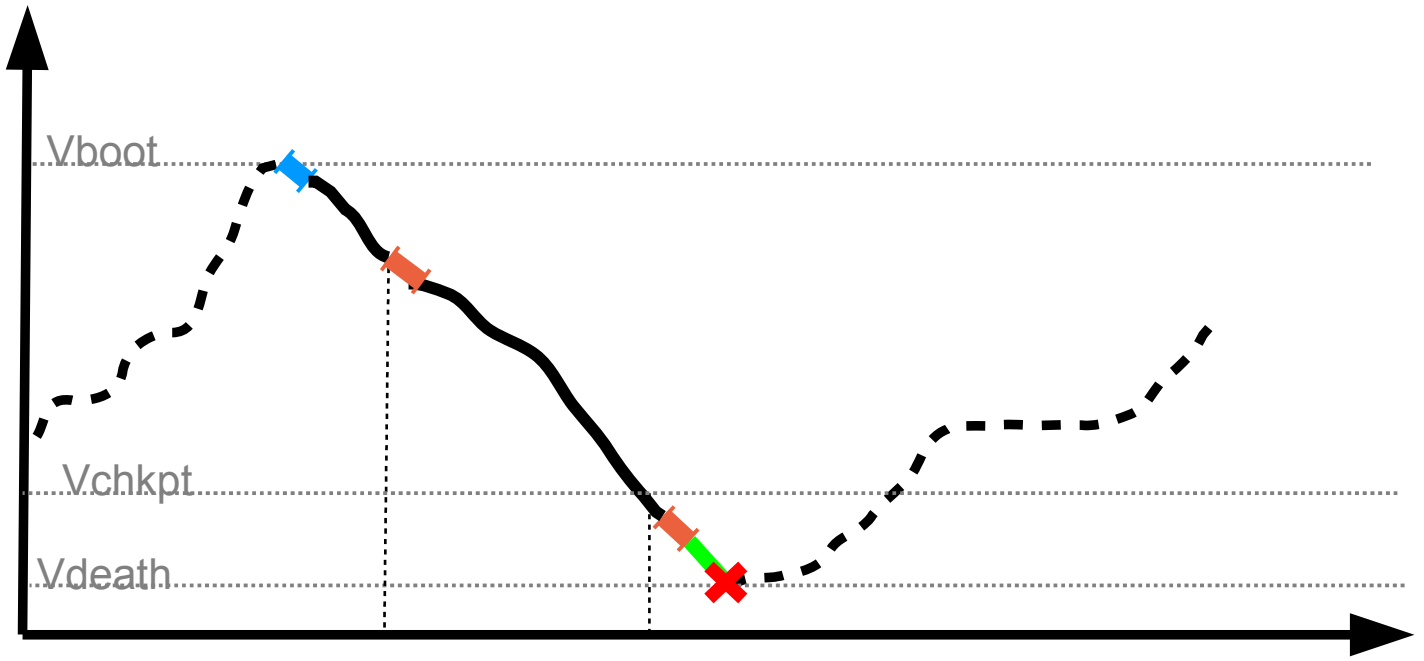
(1) Incremental Checkpointing



(2) Monitoring system's energy

2 timer based methods:

- Linear extrapolation
- Dynamic adaptation



Plan

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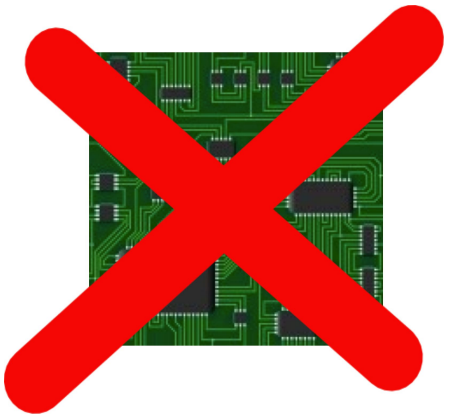
Evaluation platform

We want a hardware platform with :

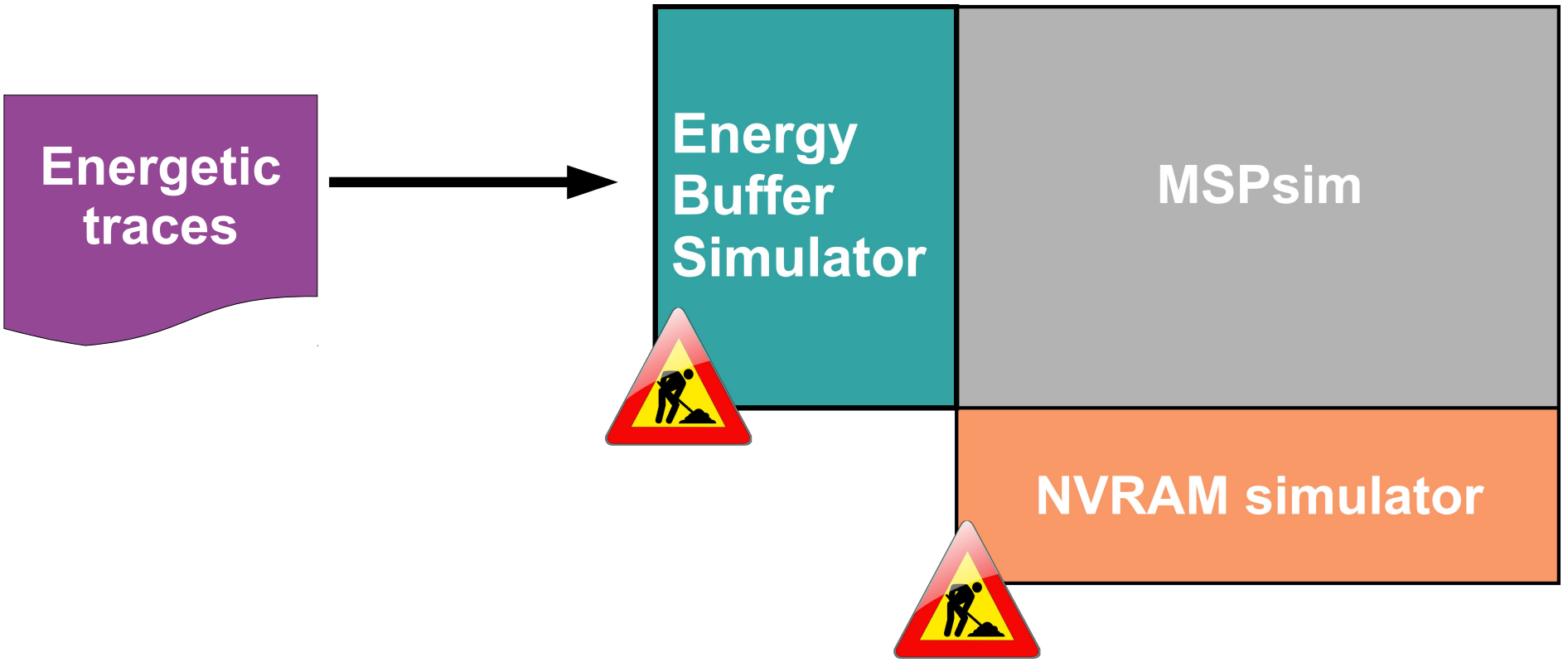
- SRAM + NVRAM memory architecture
- Energy buffer
- Energy harvester



Simulation

→ reproducibility
→ exploration

Evaluation platform



Preliminary results

- Benchmarks: crc 1e5 rsa
  Lifecycles 4 3 10
- Checkpointing ratio: 83% 70% 23%
  → Incremental checkpointing ✓
- Overhead: 12% 9% 53%
  → Timer driven ✓

Conclusion & Perspectives

- Incremental checkpointing ✓
- Timer driven ✓

We are currently working on :

- Learn the checkpointing threshold
- Improve our NVRAM models
- Improve our energetic model
- Diversify our benchmarks
- Design a real platform

NVRAM characteristics

Technology	Min. cell size(F)	Endurance (cycles)	Read latency (ns)	Write latency (ns)
SRAM	150	–	2	2
STT-MRAM	20	10^{16}	5	5–30
pSTT-MTRAM	–	–	3	3
TAS-MRAM	–	10^{12}	30	30
NAND	4	10^{4}	100E3	1E6
NOR	10	10^{5}	15	1E3
FeRAM	22	10^{12}	40	65
RRAM	30	10^{5}	100	100
PCMM	4	10^{12}	12	100